HERITAGE INSTITUTE OF TECHNOLOGY

TIME TABLE

<Electronics and Communication Engineering>

M. Tech 1st Year 2nd Semester (VLSI) **SESSION: 2022-2023**

DAY	GROUP	9.00 AM – 9.55 AM	9.55 AM – 10.50 AM	10.50 AM – 11.45 AM	11.45 AM – 12.25 PM	12.25 PM – 1.20 PM	1.20 PM – 2.15 PM	2.15 PM – 3.10 PM	3.10 PM – 4.05 PM	4.05 PM – 5.00 PM	5.00 PM – 5.55 PM
MON	GR. 1	L/VLSI 5242/AK/ICT 614	L/VLSI 5242/AK/ICT 614	L/VLSI 5232/SP/ICT 614		Remedial l/ICT 614	MENTORING/ ICT614				
	GR. 2										
TUE	GR. 1	L/VLSI 5201/KM/ICT 614	L/VLSI 5201/KM/ICT 614	L/VLSI 5232/SP/ICT 614		L/VLSI 5241/AS/ICT 614	L/VLSI 5241/AS/ICT 614	LAB/VLSI 5252 / AMB + SP / ICT 602/PS*			
	GR. 2										
WED	GR. 1	L/VLSI 5241/AS/ICT 614	L/VLSI 5241/AS/ICT 614	L/VLSI 5201/KM/ICT 614		L/VLSI 5202/KD/ICT 614	L/VLSI 5202/KD/ICT 614				
	GR. 2										
THU	GR. 1	L/VLSI 5232/SP/ICT 614	L/VLSI 5232/SP/ICT 614	L/VLSI 5242/AK/ICT 614		LAB/VLSI 5251 / KM / ICT 602/AR*					
	GR. 2										
FRI	GR. 1	L/VLSI 5202/KD/ICT 614	L/VLSI 5202/KD/ICT 614	L/VLSI 5201/KM/ICT 614		L/VLSI 5242/AK/ICT 614					
	GR. 2										

To be Effective from 9th January, 2023

A minimum of 75% attendance is mandatory for being eligible to sit for the End-Semester Examination

Students should target 100% attendance

Rajib Ranjan Pal.
Asima Adak

Member **HOD** **Principal**

HERITAGE INSTITUTE OF TECHNOLOGY

TIME TABLE

<Electronics and Communication Engineering>

M. Tech 1st Year 2nd Semester (VLSI) **SESSION: 2022-2023**

Faculty Details:

INITIALS	FULLNAME	DEPT
AS	Prof. Anindya Sen	ECE
KD	Prof. Krishanu Datta	ECE
KM	Prof. Kasturi Mukherjee	ECE
SP	Prof. Srabanti Pandit	ECE
AK	Prof. Atanu Kundu	ECE
AMB	Prof. Amrita Banerjee	ECE

TA Details:

INITIALS	FULLNAME	DEPT
PS	Mr. Pritam Sahu	ECE
AR	Ms. Aditi Ray	ECE

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<Electronics and Communication Engineering>

M. Tech 1st Year 2nd Semester (VLSI) SESSION: 2022-2023

COURSE STRUCTURE:

Sl. No.	Course Type	Code	Course Title	Contact Hours/Week				Credits
				L	T	P	Total	
1	Professional core 3	VLSI5201	Analog VLSI IC Design	3	0	0	3	3
2	Professional core 4	VLSI5202	VLSI Design, Testing and Verification	3	0	0	3	3
3	Professional Elective PE-3	VLSI5231 VLSI5232	Elective III (1) Memory Technologies (2) Low Power VLSI Design	3	0	0	3	3
4	Professional Elective PE-4	VLSI5241 VLSI5242	Elective IV (1) Advanced VLSI Processor (2) Advanced Nano Devices	3	0	0	3	3
5		VLSI5293	Term Paper and Seminar	0	0	4	4	2
6	Aud 2	Any one subject from Elective3 or Elective4 buckets	Audit Course – 2	2	0	0	2	0
Total of Theory				14	0	4	18	14

B. Practical								
1	Professional Core Lab3	VLSI5251	Analog VLSI IC Design Lab	0	0	4	4	2
2	Professional Core Lab4	VLSI5252	VLSI Design, Testing and Verification Lab	0	0	4	4	2
Total of Practical				0	0	8	8	4
Total of Semester				14	0	12	26	18

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Asima Adak

Member

HOD

Principal